IN THE CLAIMS:

Please cancel claims 7 and 8. **Please also amend** claims 1 and 19, and add new claims 22-34, as shown in the complete list of claims that is presented below.

1. (currently amended) A serial bus data control device for use with communication equipment to receive ~~two or more~~ packets sent through a serial bus and each ~~being composed of~~ having a header, actual data positioned subsequently to said header and a footer positioned subsequently to said actual data, comprising:

a preprocessing section to recognize ~~each of said two or more~~ packets received through said serial bus and to divide ~~at least~~ said header, actual data and footer contained in each of said recognized packets into ~~two or more~~ pieces of unit length data each having a predetermined data length; and

a storing section, coupled to said preprocessing section, to temporarily ~~store at least~~ said headers, actual data, and footers contained in ~~each of said~~ packets recognized by said preprocessing section, said headers, actual data, and footers of a plurality of packets being stored in said storing section simultaneously;

wherein said preprocessing section is provided with an address control circuit to assign ~~a continued address of~~ addressing in said storing ~~section, at least, to said unit length data constituting said actual data contained in each of said recognized packets composed of said header, said actual data and said footer, and~~ section for said storing headings, actual data, and footer footers,